AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An array substrate of an LCD device, comprising:

a plurality of gate lines aligned on the substrate, a plurality of data lines crossing the gate lines to form a plurality of pixel regions;

a thin film transistor located at the intersection of a gate line and a data line; and

a pixel electrode located in each pixel region,

wherein the array substrate includes ~~further comprises~~ a storage capacitor having ~~comprising:~~ a lower storage electrode across the data line and in parallel with the gate line on the same layer as the gate line[[;]], wherein the lower storage electrode divides the pixel region into two sub-regions, and a semiconductor layer ~~being formed by a diffraction pattern, said semiconductor layer~~ interposed between the lower storage electrode and the pixel electrode.

2. (Original) The array substrate of an LCD device of claim 1, wherein the pixel electrode is connected to the semiconductor layer by a through hole formed on an upper region of the semiconductor layer.

3. (Original) The array substrate of an LCD device of claim 1, wherein the semiconductor layer is inside the pixel region and is at least to be as wide as the lower storage electrode.

4. (Original) The array substrate of an LCD device of claim 1, wherein only the semiconductor layer and a gate insulating layer are interposed between the lower storage electrode and the pixel electrode.

5. (Withdrawn) A method of manufacturing an array substrate of an LCD device, comprising:

forming a gate line, a gate electrode, and a lower storage electrode on the substrate with a first mask;

sequentially forming an insulating layer, a semiconductor layer, an impure semiconductor layer, and a metal layer on the gate line, the gate electrode, and the lower storage electrode;

etching the metal layer and the impure semiconductor layer with a second mask to form a data line and a source/drain electrode, thereby exposing the semiconductor layer on the lower storage electrode;

forming a protection layer on the data line, the source/drain electrode, and the exposed semiconductor layer;

etching the protection layer with a third mask to form a contact hole and a through hole above a part of the drain electrode and the exposed semiconductor layer, and depositing a transparent electrode thereon; and

patterning the transparent electrode with a fourth mask so as to electrically connect the transparent electrode to the drain electrode through the contact hole, and forming a pixel electrode as an upper storage electrode corresponding to the lower storage electrode.

6. (Withdrawn) The method of manufacturing an array substrate of an LCD device of claim 5, wherein the exposure of the semiconductor layer above the lower storage electrode is performed by developing and etching processes using a mask of a diffraction pattern.

7. (Withdrawn) The method of manufacturing an array substrate of an LCD device of claim 5, wherein the pixel electrode is connected to the semiconductor layer by the through hole formed above the exposed semiconductor layer.

8. (Withdrawn) The method of manufacturing an array substrate of an LCD device of claim 5, wherein the exposing of the semiconductor layer above the lower storage electrode comprises:

removing a part of the photoresist deposited on the upper region of the semiconductor layer by light coming through a mask of a diffraction pattern;

removing the partly removed photoresist by an ashing process;

removing a metal layer above the semiconductor layer by performing a dry etching process for the removed photoresist region; and

removing the impurity semiconductor layer formed under the removed metal layer by a dry etching process.

9. (Currently Amended) An array substrate of an LCD device, comprising:

a gate line, a gate electrode, and a lower storage electrode~~, and an upper storage electrode~~ on the substrate;

an insulating layer~~,~~ on the substrate having the gate line, gate electrode, and lower storage electrode;

a semiconductor layer ~~exposed~~ on [[said]] the lower storage electrode~~;, an impure semiconductor layer as a source/drain electrode, and a metal layer as~~

a data line on the substrate having the insulating layer ~~on the gate line, the gate electrode, and the lower storage electrode~~;

a protection layer on the substrate having [[on]] the data line, ~~the source/drain electrode, and the exposed semiconductor layer;~~ the protection layer having a contact hole ~~and a through hole~~ above a part of the ~~drain electrode and the exposed~~ semiconductor layer; and

a pixel ~~transparent~~ electrode on [[said]] the protection layer, wherein the pixel electrode contacts the top of the semiconductor layer,

wherein said gate line and data line cross to form a pixel region, and wherein the lower storage electrode is parallel to the gate line and divides the pixel region into two sub-regions~~; and~~

~~wherein the transparent electrode is connected to the drain electrode through the contact hole~~.

10. (Currently Amended) The array substrate of an LCD device of claim 9, wherein the pixel electrode is connected to the semiconductor layer by the through hole above the ~~exposed~~ semiconductor layer.

11. (Original) The array substrate of an LCD device of claim 9, wherein the semiconductor layer is inside the pixel region and is at least as wide as the lower storage electrode.

12. (Original) The array substrate of an LCD device of claim 9, wherein only the semiconductor layer and a gate insulating layer are interposed between the lower storage electrode and the pixel electrode.